LISTING OF THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

1. (Previously Presented) A coupling arrangement for coupling a semiconductor device chip to different models of semiconductor device testers, the arrangement comprising:

a mother board electrically compatible with each of respective test heads of the different testers, wherein the mother board includes input terminals located at a peripheral edge and adapted to receive electrical signals from the testers, and connectors located at a central portion of the mother board and adapted to transmit the electrical signals; and

a device under test (DUT) board connectable between the mother board and the semiconductor device chip to be tested by one of the different models of tester, and adapted to receive the electrical signals from the mother board.

2. (Original) The coupling arrangement of claim 1 further comprising:

a load board loading unit to mechanically bind the mother board to any one of the test heads.

3. (Original) The coupling arrangement of claim 1, wherein the mother board provides signal paths for mixed signals, respectively.

4. (Original) The coupling arrangement of claim 1, wherein a plurality of locking units are placed on the mother board for mechanically connecting the DUT board to the mother board.

5. (Previously Presented) The coupling arrangement of claim 1, wherein input terminals for test signal paths clustered into a smaller area on an opposite side of the mother board from the peripheral input terminals and the centralized connectors.

6. (Previously Presented) The coupling arrangement of claim 4, wherein the plurality of locking units has the same shape regardless of the particular type of tester.

7. (Previously Presented) The coupling arrangement of claim 1, wherein the DUT board includes vertical type relays.

8. (Previously Presented) A method of making one or more test connections between a semiconductor device chip and different models of semiconductor device testers that are each operable upon the semiconductor device chip, the method comprising:

providing a mother board electrically compatible with each of respective test heads of the different testers;

providing a device under test (DUT) board connectable between the mother board and the semiconductor device chip to be tested;

coupling any one of the respective test heads to the mother board;

coupling the DUT board to the mother board; and

coupling the semiconductor device chip to the DUT board.

9. (Previously Presented) The method of claim 8, further comprising:

mechanically binding the mother board to the test heads via a load board loading unit.

10. (Original) The method of claim 8, wherein the mother board provides signal paths for different models of testers of mixed signals, respectively.

11. (Original) The method of claim 8, further comprising binding the DUT board to the mother board via a plurality of locking units.

12. (Previously Presented) The method of claim 8, further comprising:

arranging the input terminals at a first side of the mother board to have test signal paths distributed azimuthally around the center thereof, and arranging a second side of the mother board to have terminals for test signal paths, respectively, gathered into a relative smaller predetermined area.

13. (Previously Presented) The method of claim 12, wherein the predetermined area is arcuate in shape.

14. (Original) The method of claim 8, further comprising electrically connecting test signal paths through the mother board to test signal paths on the DUT board via aligning conductive terminals.

15. (Previously Presented) A test system adapted to test a semiconductor device chip, comprising:

a tester adapted to test mixed signals of the semiconductor device chip;

a mother board including input terminals located at a peripheral edge of the mother board and adapted to receive electrical signals from the tester, and connectors located at a central portion of the mother board and adapted to transmit the electrical signals; and

a device under test (DUT) board connectable between the mother board and the semiconductor device chip to be tested by one of the different models of tester, and adapted to receive the electrical signals from the mother board.

16. (Previously Presented) The system of claim 15, further comprising:

a test head;

a signal cable connecting the test head with the tester; and

a load board loading unit to mechanically bind the test head with the mother board.

17. (Previously Presented) The system of claim 15, further comprising a locking unit to lock the mother board with the DUT board.

18. (Currently Amended) The system of claim ~~14~~ 15, wherein the input terminals are provided at a first side of the mother board to have test signal paths distributed azimuthally around the center thereof, and wherein the input terminals are provided in a second side of the mother board and gathered into a relative smaller predetermined area.

19. (Currently Amended) The system of claim ~~14~~ 15, wherein the DUT board is adapted mount more than one semiconductor chip.

20. (Previously Presented) The method of claim 8, wherein the mother board includes input terminals located at a peripheral edge to and adapted receive electrical signals from the testers, and connectors located at a central portion of the mother board and adapted to transmit the electrical signals.